AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

1 (Currently amended). A method of π/4-shift QPSK modulation comprising:

providing a portion of an address in a direct order ~~addressing symbols~~ from a Precursor section of a register to a first memory portion and in a reversed order from a Postcursor section of said register to a second memory portion at odd times; and

providing said portion of the address in the direct order ~~addressing symbols~~ from said Precursor section to said second memory portion and in the reversed order from said Postcursor section to said first memory portion at even times ~~by using reversed addressing for Postcursor symbols in accessing the said first and second memory portions~~.

2 (Currently amended). The method of claim 1, further comprising:

successively incrementing the portion of the address indicated by the Precursor section of the register by a number of storing locations ~~equal~~ according to ~~said~~ a predetermined number of samples, and successively decrementing the address indicated by the Postcursor section of the register by a number of storing locations ~~equal~~ according to said predetermined number of samples.

3 (Original). The method of claim 2, wherein the first memory portion and the second memory portion are adapted to Look Up Tables format.

4 (Currently amended). The method of claim 3 comprising: ~~, wherein~~

adapting the ~~shift~~ register ~~is adapted~~ to ~~comprise~~ include n symbols~~,~~ wherein, the Precursor ~~comprises~~ includes n/2 of said n symbols and the Postcursor ~~comprises~~ includes ~~the remaining~~ n/2 of said n symbols.

5. Canceled

6 (Currently amended). The method of claim 4, further ~~comprises~~ comprising:

defining a transfer function of the modulator by an array of characteristic coefficients;

computing for ~~each~~ a possible inputted symbol sequence, a predetermined number of sample values, said sample values being the sum of the products of said symbol sequence multiplied by said coefficients; and

providing an output of said modulator by an addition of the Precursor sum-of-products and Postcursor sum-of-products.

7 (Currently amended). The method of claim 6, ~~comprises~~ comprising:

storing said sums-of-products said first memory portion and said second memory portion.

8 (Currently amended). The method of claim 7, ~~comprises~~ comprising:

defining an amplitude value of symbols inputted at odd times by combinations of an at least two bits and an amplitude value of symbols inputted at even times by an at least one bit, and feeding the resulting symbols to said ~~shift~~ register.

9. Canceled

10 (Original). The method of claim 1, further comprising:

assigning one symbol in the Precursor section and one symbol in the Postcursor section as sign symbols to said sections correspondingly; and

forming the address to the corresponding memory portion from the symbols coming from the corresponding register in accordance with the sign of said sign symbols.

11 (Currently amended). The method of claim 10, comprising: selecting ~~wherein each of said sign symbols is selected~~ from the symbols represented by one bit a sign symbol.

12 (Original). The method of claim 11, further comprising:

when a sign bit is negative, forming the address to the corresponding memory portion from all symbols coming from the corresponding register section except the sign symbol, reversing the sign of each symbol in the corresponding register section, and further reversing the sign of the outputs from the corresponding memory portion;

otherwise forming the address to the corresponding memory portion from all symbols coming from the corresponding register section except the sign symbol.

13 (Currently amended). The method of claim 12 comprising ~~, wherein the first and second memory portions are integrated~~ integrating the first and second memory portions in a single memory unit.

14 (Currently amended). An $\pi/4$-shift QPSK modulator comprising:

~~at least one shift~~ a register ~~comprises at least one~~ having a Precursor section to provide a first portion of an address in a direct order to a first memory portion and ~~at least one~~ a Postcursor section to provide a second portion of the address in a reveres order to a second memory portion; and

~~at least one address convertor which is adapted to convert the symbols from~~ a control to alternate the first and second portions of the address provided by the Precursor section and the Postcursor section of said register ~~alternately~~ to ~~a~~ the first and ~~a~~ second memory portions according to even and odd times ~~and from the Postcursor section of said register alternately to said second and first memory portions~~.

15 (Currently amended). The modulator of claim 14, further ~~comprises~~ comprising:

~~at least one~~ a counter ~~adapted~~ to increment and decrement ~~the~~ a least significant bits of the address; and

~~a plurality of~~ two or more multiplexers ~~adapted~~ to select outputs of the Precursor section of the register to form ~~an~~ the first portion of the address to ~~one~~ the first memory portion, and the Postcursor section of the register to form ~~an~~ the second portion of the

address to the second memory portion, while reversing the order of the Postcursor symbols, said selection is alternated at even and odd times.

16 (Currently amended). The modulator of claim 15, further ~~comprises~~ comprising:

~~at least one~~ an adder ~~adapted~~ to add a data outputted from said first memory portion to a data outputted from said second memory portion; and

~~at least one~~ a digital to analog converter ~~adapted~~ to convert the combined output to an analog output.

17 (Currently amended). The modulator of claim 15, wherein said second memory portion ~~is~~ ~~adapted~~ to integrate with unused memory locations of said first memory portion.

18 (Currently amended). The modulator of claim ~~18~~ 15, wherein the first and second portions of the addresses ~~in the memory~~ are ~~defined by a high address factor~~ most significant bits, being formed by symbols in the register, and ~~by~~ a third portion of the address is ~~low address factor~~ least significant bits, which generates in accordance with the order of sampling within the symbol.

19 (Currently amended). The modulator of claim 18 wherein, said ~~low address~~ least significant bits are provided by said counter.

20. Canceled.

21 (Currently amended). The modulator of claim ~~16~~ 15 wherein, ~~the at least one~~ said counter is adapted to provide the ~~L~~least ~~S~~significant ~~B~~bits ~~of the address comprises~~ includes an over sampling counter.

22 (Original). The modulator of claim 15, further comprising:

a bits to symbols conversion unit for converting a sequence of bits into a sequence of symbols represented alternately by one and two bits.

23 (Currently amended). The modulator of claim 22, wherein said ~~shift~~ register is adapted to receive said sequence of symbols.